REMARKS

Claim 3

Claim 3 was rejected as being anticipated by Takenouchi (U.S. Patent No. 5,744,758).

Takenouchi does not disclose laminating a first prepreg and a copper foil on a surface of a second conductive layer, laminating a second prepreg on a surface of the n-th conductive layer, and simultaneously press-bonding the first and second prepregs, the copper foil, the second to n-th conductive layers, and the insulating layers to form a multilayer substrate having an odd number n of insulating layers) this is supported on page 10, lines 17-24 of the specification), as recited in amended claim 3. Rather, Takenouchi discloses laminating a thermosetting resin film 14 on a thermoplastic resin layer 16 to form a substrate 12 and heat-pressing a suitable number of substrates 12 (see column 7, line 59 - column 8, line 36). That is, Takenouchi heat-presses substantially the same materials of resin. In contrast, the present invention press-bonds the insulating layers and prepregs (the prepregs being different from the insulating layers). Since the present invention simultaneously press-bonds two prepregs, it provides the benefit that thermal pressure is uniformly applied to both sides of the insulating layers, thereby preventing warping from occurring in the insulating layers. Accordingly, the present invention of claim 3 distinguishes over Takenouchi.

Claim 7

Claim 7 also was rejected as being anticipated by Takenouchi (U.S. Patent No. 5,744,758).

Takenouchi does not disclose forming conductive layers on a plurality of insulating layers respectively, wherein each of the insulating layers is selected from a group comprising resin base materials containing a single synthetic resin substance, resin base materials containing synthetic resins and inorganic fillers, and cloth base materials containing synthetic resins and inorganic cloth (this is supported on page 17,

lines 5-9 of the specification), as recited in amended claim 7. Accordingly, the present invention of claim 7 distinguishes over Takenouchi.

Claims 1 and 2

Claims 1 and 2 were rejected as being unpatentable over Takenouchi in view of Ishii (U.S. Patent No. 5,435,877).

Neither Takenouchi nor Ishii disclose that (1) a first to (n-1)-th insulating layers has as least one of through holes with a plating film formed on the wall thereof to connect the conductive layers (this is supported on page 31, lines 8-10 of the specification), and (2) a central insulating layer of the odd number of insulating layers prevents warping from occurring in the printed wiring, as recited in amended claim 1. Since the plating film is formed on the wall of the at least one through hole, the plating film is stably formed and the electric connectivity between conductive layers is stabilized. Takenouchi, on the other hand, discloses a multilayer circuit board that includes a via-hole 19 through a thermosetting resin film 14 filled with a plated metallic layer 32 and a thermoplastic resin paste containing electro conductive material 34 formed on the plated metallic layer 32. Ishii discloses a prepreg comprising glass a glass cloth. Accordingly, the references collectively do not disclose all of the elements of claim 1 and, thus, the present invention of claim 1 is not obvious over Takenouchi in view of Ishii.

Claim 2 depends from claim 1 and, therefore, distinguishes over the prior art for the same reasons.

Claim 10

Claim 10 also was rejected as being unpatentable over Takenouchi in view of Ishi (U.S. Patent No. 5,435,877).

Claim 10 depends from independent claim 7 which was already discussed above. It distinguishes over the combination of Takenouchi and Ishi for the same reasons discussed above with respect to claim 7. Ishi does not add the teachings lacking from Takenouchi discussed above in connection with claim 7 (Ishi was cited for other reasons). Specifically, neither Takenouchi nor Ishii disclose forming conductive

layers on a plurality of insulating layers respectively, wherein each of the insulating layers is selected from a group comprising resin base materials containing a single synthetic resin substance, resin base materials containing synthetic resins and inorganic fillers, and cloth base materials containing synthetic resins and inorganic cloth, as recited in amended claim 7.

Claim 4

Claim 4 was rejected as being unpatentable over Sisler (U.S. Patent No. 5,010,641) in view of Del (U.S. Patent No. 4,180,608).

Neither Sisler nor Del disclose that (1) an internal insulating layer comprises two or more internal insulating layers of glass cloth-reinforced prepreg containing 30 to 70% by weight of glass cloth, and (2) an external insulating layer comprises synthetic resins and inorganic fillers or synthetic resin single substances (this is supported on page 17, lines 5-7 of the specification), as recited in amended claim 4. The glass cloth-reinforced prepreg reduces coefficient of water absorption of the internal insulating layer and reduces the absolute amount of water to be contained in the internal insulating layer, thereby reducing the amount of water vapor collected between the layers, which increase interlayer adhesion, even though a printed wiring board is subjected to some thermal processes (e.g. plating process, dry process, curing process of a solder resist, reflowing a solder). Furthermore, since the external insulating layer comprises synthetic resins and inorganic fillers or synthetic resin single substances and does not comprise glass cloth, it facilitates formation of fine patterns with relatively small via holes. Neither Sisler nor Del disclose the combination of the prepreg and the resin. Accordingly, the present invention of claim 4 is not obvious over Sisler in view of Del.

Claims 15 and 18

Claims 15 and 18 were rejected as being unpatentable over Swamy (U.S. Patent No. 5,541,368) in view of Kamperman (U.S. Patent No. 5,734,560).

Neither Swamy nor Kamperman discloses that a metal plating film covers a wall of the interconnecting through hole and the bottom of the interconnecting through hole defined by a covering pad (this is supported on Figs. 38 and 39), as recited in amended

claim 15. Since the plating film covers the wall and bottom of the through hole, the rigidity of the printed wiring board is secured and warping is prevented in the printed wiring board, thereby preventing a conductive layer from projecting from a through hole, securing electric connectivity between conductive layers, and securing the flatness of the surface layer. Accordingly, a stable connection between the board and components mounted thereon is maintained. Furthermore, early deterioration of the board is prevented when it is subjected to a reliability test, such as a heat shock cycle test. Swamy discloses a through hole 44 and a solder ball 24 for an external connection. Kamperman discloses a through hole and a solder ball 13 for an external connection. Accordingly, the present invention of claim 15 is not obvious over Swamy in view of Kamperman.

In view of the foregoing amendments and remarks, this application is now in condition for allowance. Applicant respectfully requests the Examiner to issue a Notice of Allowance at the earliest possible date. The Examiner is invited to contact Applicant's undersigned counsel by telephone call in order to further the prosecution of this case in any way.

Respectfully submitted,

October 27, 2005

Theodore Naccarella, Reg. No. 33,023
Synnestvedt & Lechner LLP
1101 Market Street
2600 Aramark Tower
Philadelphia, PA 19107-2950
Tele: (215) 923-4466
Fax: (215) 923-2189

TXN:pmf

M:\TNaccarella\CLIENTS\Onda\23128\PTO\Reply to action of 6-24-05.doc